Direct-Write Technology for a Cable-free Digital Sensor-Bus

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Motivation for Research

- SHM improves reliability, safety & readiness @ reduced costs
  - adds weight, consumes power & computational bandwidth
  - traditional cables susceptible to EMI, durability & signal attenuation
  - scaling SHM for large-area coverage has presented challenges
- Local sensor digitization (US patent 7,373,260 & other pend.)
  - convert analog signals into digital data at point-of-measurement (POM)
  - eliminates EMI & attenuation issues
  - enables serial sensor connections to minimize total cable length
  - digital sensor-bus alone not sufficient, cable harness durability concerns
  - wireless transmission infeasible, power requirements & regulatory issues

Direct-Write (DW) Technology

- Simple basic principal behind all DW methods
  - fine electrically conductive & insulative traces selectively deposited
  - directly onto structure or onto an intermediary substrate
  - conformal traces create a multifunctional structural component
  - CAT-6 equivalent weighs < 25 g per meter of length
- There are multiple DW methods commercially available
  - Plasma Flame Spray (PFS) of copper & ceramic (Mesoscribe)
  - Jetted Atomized Deposition (JAD) of silver nano-ink & epoxy (Optomec)
- Extensively tested by Boeing
  - shown DW traces to be extremely resilient to mechanical loading
  - designed impermeable to environmental factors with an encapsulant
  - demonstrated in a large scale production environment, FAA approved

Benchmark System

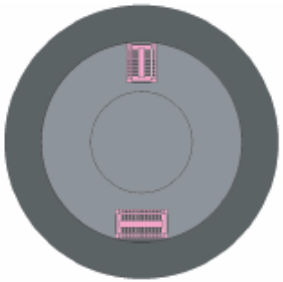
- Present research explored the patent pending concept of a "cable-free" digital sensor-bus for SHM using DW

- Selected hypothetical SHM system for design process
  - 100 digital sensor nodes
  - distributed over 100 m total length (straight line or meandering over grid)
  - sensors spaced by 0.5 m along bus
  - based on requirements derived from Ares V composite interstage

- Design process developed & executed
  - appropriate DW methods selected
  - conductive & insulative trace & layer dimensions were iteratively chosen
  - configuration to achieve desired transmission characteristics identified
  - proof-of-concept validation experiment conducted

Physical Connectivity

- SHM nodes considered
  - Intelli-Connector™ digital SHM node selected for POM digitization
  - next generation Intelli-Connector™ HS designed in parallel w/sensor-bus



- Hardware Compatibility
  - *communication*: differential controller area network (CAN), requires 2 parallel conductors (high & low) w/impedance 100-130 Ω
  - *synchronization*: high-speed RS-422 digital differential sync protocol, requires 2 parallel conductors (high & low) w/impedance 100-130 Ω
  - *power*: 108 mA max current draw, standby current draw of 30 mA; 3.5 A benchmark assumes 1 exciting node & 6 sensing nodes at a time @ 28V
  - *shielding*: parallel shield traces should separate CAN & sync traces, top/bottom layers couples untwisted pairs & protects against EMI

Conductor Break-Out Methods

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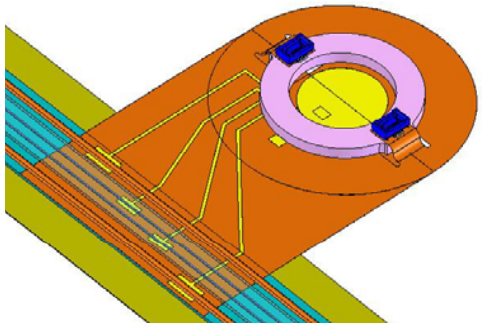
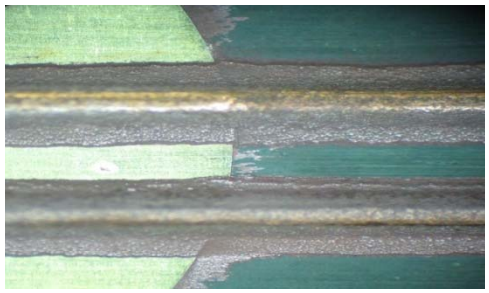
- Connectors installed over DW traces
  - creating 3-D via's are very difficult
  - traces are very close together



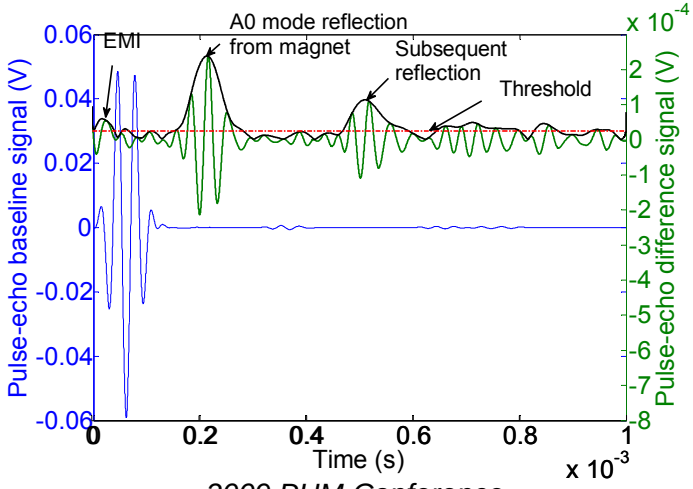
- Bonding flex directly over DW traces
  - alignment complexities
  - delamination conerns at "step" from traces



- Deposit DW traces over flexible circuit stub ("flex-tail")
  - flex-circuit already conceived for HS node power/comm connection
  - bonded to structure during DW integration, selectively exposed copper
  - durable & reliable solution with minimum mass impact
  - experimentally validated & debugged process
  - can also add connector to flex-tail for compatibility with other sensors

SHM Method Compatibility

- Investigate effect of DW traces on wave propagation for SHM
  - concerns for GW scatter points, can change phase & amplitude
  - experiment conducted to observe interaction of GW w/DW traces
- CFRP plates measuring 75 x 75 x 0.25 cm thick tested
  - instrumented w/3 PZT sensor pairs bonded opposite to pair of DW traces
  - catch signals indicated some attenuation but no significant phase change
  - echo signals found a small but detectible reflection from DW traces
  - overall DW did not effect detection, locating or range (40 cm here)



Electrical Compatibility

- Physically connecting hardware to DW sensor-bus not sufficient
  - communication & sync traces must match prescribed impedance
  - power lines must carry required current over desired total length
  - shield layers need to be sized to provide the desired protection
- Node # & bus length dictated by materials, geometry & spacing
  - collect toolset of equations to be used for design optimization
  - measure the electrical properties of common DW materials
  - resistance – function of material conductivity & trace area
  - impedance – function of insulator dielectric, trace geometry & spacing
- Applicable standards
  - MIL-STD-275E & IPC-2221: generic standards on printed board design
  - MIL-STD-461F: requirements EMI characteristics of equipment
  - MIL-STD-810E: environmental conditions for airborne equipment

Communication & Sync Traces

- Spice simulation model built to optimize CAN configuration
  - theoretical values for good conductors used
  - true values for CAN controller elements of SHM nodes used
  - input of high/low CAN pulse pair, differential voltage output for final node
- For digital communication key parameter is impedance
  - very complex function, generally need small traces close together
  - function of conductor trace width, spacing, thickness & conductivity
  - function of in-plane shield trace & out-of-plane shield layer spacing
  - function of insulator dielectric constant between conductors and shields
- Traces determined to be 0.25 mm x 10 µm thick w/0.5 mm pitch
  - much finer than PFS is capable of depositing
  - only JAD considered for CAN & sync traces (same impedance required)

JAD Experimental Characterization

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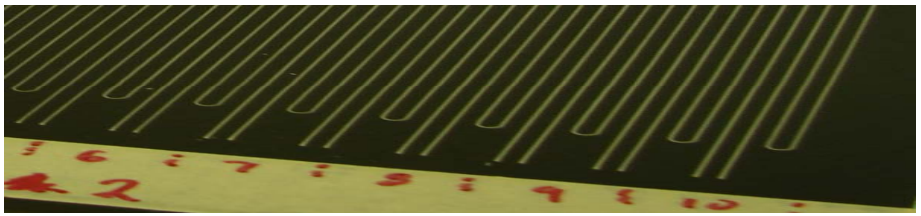
- Experimental procedure conducted to characterize JAD
  - measure conductivity of silver nano-ink traces
  - verify tolerances & manufacturing capabilities of method
- JAD was capable of achieving required geometry
  - resistance 10^3 x expected/desired values (1 kΩ/m compared to 1 Ω/m)
  - thickness was issue, assume better capabilities in near future
- Screen-printing process developed for present research
  - silver epoxy spread over chemical-etched steel shim templates
  - much thicker silver traces can be patterned than current JAD
  - finer pitch traces possible than PFS (no overspray)
  - updated traces determined to be 0.33 mm x 125 µm thick w/1.5 mm pitch



Power Traces

- Power trace design dominated by 3 factors
  - maximum voltage carrying capabilities (needs to be at least 28 V)
  - maximum current carrying capabilities (needs to be at least 3.5 A)
  - material resistivity
- Material resistivity dictates how many total nodes can be connected to the bus over what total length
- Only PFS could meet constraints
  - large area traces
  - high conductivity

PFS Trace Voltage & Current Limits

- Minimum trace spacing
  - 0.1 mm for 0 to 50 V_{DC} or V_{AC}
  - Type A5 – assemblies w/external conductors & conformal coating
  - Table I in 4A in MIL-STD-275E and Table 6-1 in the IPC-2221 standard
- Minimum conductor cross sectional area
  - 0.16 mm^2 for 3.5 A with a 2x factor of safety
  - for external etched copper conductors
  - Figure 4A in MIL-STD-275E and Figure 6-4 in the IPC-2221 standard
- Assumptions
  - 100 nodes connected to the power trace, 1 exciting & 6 sensing at a time
  - nodes are spaced ½ m (~1.5 feet)
  - power dissipated in the nodes is constant regardless of voltage
  - traces have a conductivity equal to 58 x 10^6 S / m (IACS at 20°C)

PFS Trace Total Node/Length Limit

- Power trace resistance limits total # nodes and/or bus length
  - system treated as large circuit diagram solved by Kirchhoff's laws
  - 93 nodes consuming 0.8W in standby & 7 nodes consuming 3W sensing
  - each trace between nodes modeled as small resister
  - assume trace conductivity equal to 58×10^6 S/m (IACS at 20°C)
  - equations dictated minimum cross-sectional area of ~1 mm^2

Trace area	0.58 mm^2 (1.5 x 0.3 mm)	0.77 mm^2 (1.5 x 0.5 mm)	1.16 mm^2 (3.0 x 0.5 mm)
Resistance per length	30.0 mΩ / m	22.2 mΩ / m	14.8 mΩ / m
Bus input voltage	28 V_{DC}	28 V_{DC}	28 V_{DC}
Last node voltage (needs 24 V_{DC})	20.3 V_{DC}	22.8 V_{DC}	24.8 V_{DC}
Bus input current	4.2 A_{DC}	3.9 A_{DC}	3.7 A_{DC}
Bus input power	118 W	110 W	104 W
% power dissipated in traces	20 %	13 %	8 %

PFS Experimental Characterization

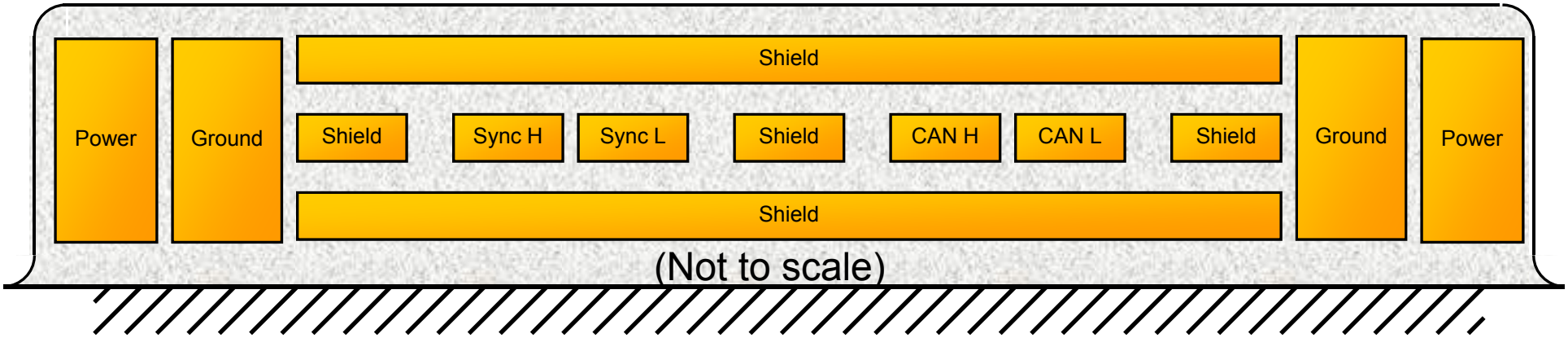
- Voltage & current limits
  - 0.1, 0.2 & 0.3 mm^2 traces deposited w/total length of ~5 m (2.5 mm pitch)
  - 40 V_{DC} power supply connected to each pair of traces, current measured
  - all traces successfully carried 9.5 A_{DC} for 5+ minutes without failure
- Conductivity measurements
  - electrical conductivity related to trace resistance by $R=L / (\sigma * A)$
  - $8x10^6$ S/m for 0.1 mm^2, $13x10^6$ S/m for 0.2 mm^2, $17x10^6$ S/m for 0.3 mm^2
  - low compared to standard due to impurities & geometry assumptions
- Consequence of lower conductivity
  - fewer nodes can exist on bus as designed
  - nodes need to be spaced closer together
  - otherwise traces will need to be re-sized

Shield Traces

- Shield layers serve to protect CAN & sync from EMI
  - 1 µm is an excellent shield against electric interference up to 1 MHz
  - 10 µm is a mild shield against magnetic interference up to 1 MHz
- Shield layer plays an important role in impedance calculation
  - if placed far enough away from traces they have little influence
  - in-plane shield traces can be neglected if pitch is same as conductors
  - out-of-plane shield cannot be neglected within reasonable geometry
  - out-of-plane shield designed to be 0.5 mm above and below conductors
  - remaining volumes between conductors & shields filled with dielectric

Overall Configuration

- Great challenge was system integration
  - maintain optimized characteristics of all elements
  - minimize overall bus geometry & mass to maintain benefits of DW
  - consider fabrication processes so that configuration could be made
- Evident neither PFS or JAD able to be exclusively used bus
  - PFS thick enough for power but too poor tolerances for communication
  - JAD accurate enough for controlled impedance but too thin for power
  - hybrid approach is necessary to achieve desired functionality

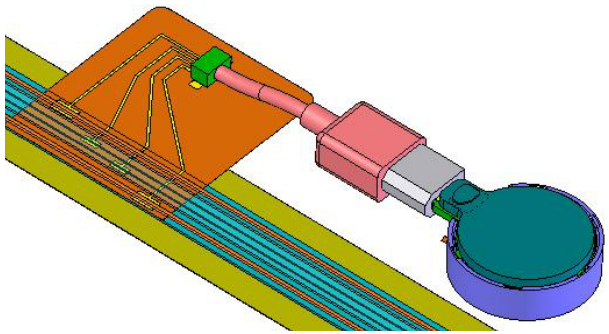


Conductor Trace Dimensions

- Communication & Synchronization
  - CAN (+/-) and sync (+/-) traces 330 µm x 125 µm thick with 1.5 mm pitch
  - size dictated by impedance requirements
- Power & Ground
  - 2 pairs of 1.25 mm x 1 mm thick with 12 mm effective pitch for 1 mm^2
  - size dictated by voltage drop per length
- Shield
  - top & bottom shield layers 10 µm thick surround traces with 1 mm pitch
  - size dictated by skin depth
- Overall dimensions
  - 1.35 cm x 1.25 mm thick
  - 25 g per meter, total of 2.5 kg for benchmark system (1.5 kg for sensors)

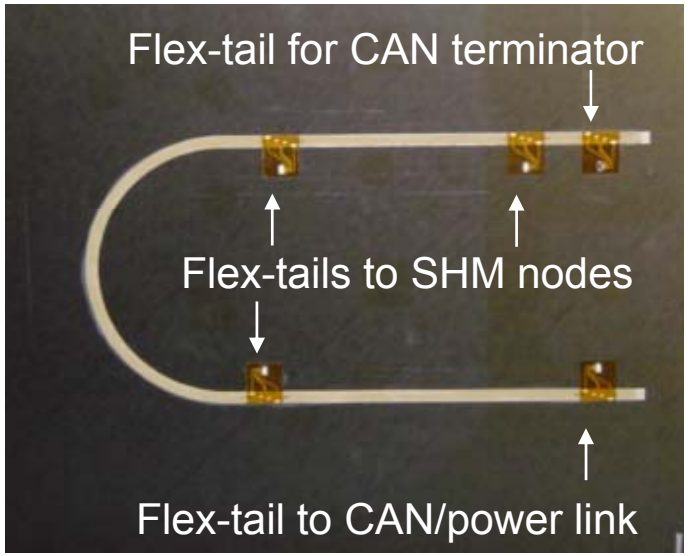
Initial Implementation

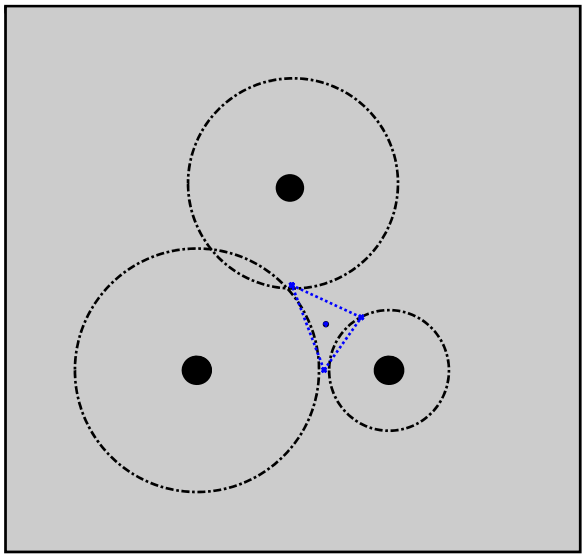
- Initial demo required deviation from eventual production design
- Physical Connectivity
  - Intelli-Connector™ connects to power & CAN through FireWire plug
  - flex-tail adapter designed to make connection for demonstration
  - Intelli-Connector™ HS sensors are directly compatible w/flex-tail design
- Electrical Compatibility
  - overall configuration minimized to demonstrate function at reduced risk
  - since CAN & sync traces require identical impedance, only CAN written
  - since 3 nodes will be used over 1 m, only 1 power pair written (0.5 mm^2)
- Silk-screen process used instead of thin JAD traces



Proof-of-Concept Demonstration

- Digital sensor-bus installed on 75 x 75 x 0.25 cm CFRP plate
  - 3 Intelli-Connector™ SHM nodes bonded in isosceles triangle formation
  - front-end connected to CAN/USB plug, aft-end to termination resistor
- Magnet to simulate damage (12.7 mm diameter x 6 mm tall)
  - no communication or power problems were encountered
  - across 10 trials without magnet no false positives reported
  - across 10 trials with magnet average error in prediction was 7.5 mm





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